Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A system, comprising:

a memory device;

a first processor that executes a first program;

a counter coupled to the memory device and the first processor, wherein a value of the counter ~~is adapted to monitor~~ is indicative of memory consumption of memory of the memory device ~~for one or more programs~~by the first program;

a second processor coupled to the memory device, the second processor executes a garbage collector ~~a plurality of processors coupled to the counter, wherein one of the plurality of processors within the system is coupled to a garbage collector adapted~~ to free a portion of unused memory in the memory device; and

wherein executing the garbage collector by the second processor is triggered based on ~~a~~the value of the counter.

2. (Original) The system of claim 1, wherein the value is a programmable threshold value, and wherein when the counter reaches the programmable value, the garbage collector is triggered.

3. (Currently Amended) The system of claim 2, wherein upon reaching the programmable threshold value, the counter sends an interrupt value to the second processor to initiate ~~, which executes~~ the garbage collector.

4. (Original) The system of claim 2, wherein a software process is regularly polling the counter to check if the predetermined threshold value has been

reached, and wherein upon reaching the predetermined threshold value, the garbage collector is triggered.

5. (Currently Amended) The system of claim 1, wherein the first processor ~~system~~ further comprises a decoder coupled to the counter, wherein upon decoding an instruction of the first program requesting memory allocation, the counter is updated with an estimated memory usage value for the instruction.

6. (Currently Amended) The system of claim 1, wherein the ~~system~~ first processor ~~further comprises a micro-sequence replacing~~ replaces an instruction of the program requesting memory allocation with a micro-sequence, wherein upon executing an instruction from the micro-sequence requesting memory allocation**[[,]]** by the first processor the counter is updated with an exact memory usage value for the instruction of the first program.

7. (Currently Amended) The system of claim 6, wherein the counter is ~~updated by a value stored~~ resides within the memory device.

8. (Currently Amended) The system of claim 1, wherein a software process is triggered by an instruction of the first program that requests memory allocation, and wherein prior to performing or requesting another memory allocation task, the software process executing on the first processor increments ~~a~~the counter indicative of the memory consumed.

9.-14. (Cancelled)

15. (Currently Amended) A system, comprising:

a first processor ~~coupled to a~~ that executes a garbage collector ~~adapted~~ to free unused memory resources ~~for one or more programs~~within a memory device;

a second processor coupled to the first processor and the memory that

executes a program that allocates memory within the memory device;

a counter coupled to the first and second processors, wherein the counter ~~is adapted to monitor~~ indicates memory consumption for the ~~one or more programs~~program; and

wherein upon surpassing a threshold value, the counter triggers the garbage collector.

16. (Currently Amended) The system of claim 15, wherein the system further comprises a decoder within the second processor coupled to the counter, and wherein the decoder provides information to update the counter.

17. (Original) The system of claim 16, wherein the decoder decodes a standard Java instruction requesting memory allocation.

18. (Original) The system of claim 17, wherein the counter is updated with an approximate memory usage value.

19. (Original) The system of claim 16, wherein the decoder decodes an instruction from a micro-sequence requesting memory allocation.

20. (Original) The system of claim 19 and wherein the counter is updated with an exact memory usage value.

21. (Currently Amended) The system of claim 15, wherein the counter is monitored periodically by a software process~~, and upon reaching the threshold value, the software process~~ that triggers the garbage collector when the counter reaches a predetermined threshold, and wherein the software process executes in at least one selected from the group consisting of: the first processor; or the second processor.

22. (Currently Amended) The system of claim 15, wherein the first processor is a main processor and the second is a processor that directly executes at least some Java bytecodes .

23.-24. (Cancelled)

25. (Original) The system of claim 15, wherein the system is a cellular telephone.

26. (New) A computer-readable media comprising a plurality of instructions that, when executed by a processor, cause the processor to:

monitor memory consumption of a memory device for one or more programs executed in a first processor;

trigger a garbage collector program in a second processor to free a portion of the memory upon surpassing a threshold memory consumption; and

update a memory usage counter after retrieving a portion of the memory.

27. (New) The computer-readable medium as defined in claim 26 wherein when the processor monitors memory consumption, the instructions cause the processor to monitor memory consumption of the one or more programs on the first processor being the same processor on which the plurality of instructions execute.

28. (New) The computer-readable medium as defined in claim 26 wherein when the processor monitors memory consumption, the instructions cause the processor, being the second processor, to monitor memory consumption of the one or more programs on the first processor.

29. (New) The computer-readable medium as defined in claim 26 wherein when the processor monitors memory consumption, the instructions cause the

processor to monitor the value of a counter.

30. (New) The computer-readable medium as defined in claim 29 wherein when the processor monitors the counter the instructions cause the processor to monitor the counter in the first processor.